PATENT
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#14 Appeal Br. EOT. (1) 2/1/02 a

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellants	:	Takumi OKAUE et al.
Serial No.	:	09/467,221
Filed	:	December 20, 1999
For	:	**EXTERNAL STORAGE APPARATUS AND CONTROL APPARATUS THEREOF, AND DATA TRANSMISSION RECEPTION APPARATUS**
Examiner	:	L. Taylor ~~D. Felten~~
Art Unit	:	2876

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231, on October 30, 2001.

William S. Frommer, Reg. No. 25,506
Name of Applicant, Assignee or Registered Representative

Signature

October 30, 2001
Date of Signature

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BOARD OF PATENT APPEALS AND INTERFERENCES

APPEAL BRIEF OF APPELLANTS

Board of Patent Appeals and Interferences
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Transmitted herewith in triplicate is Appellants' Brief in support of the appeal from the Final Rejection dated January 31, 2001 in the above-identified application. A one month extension of time is requested.

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02 FC:120 320.00 OP

A check in the amount of $320 is attached in payment of the required fee set forth in 37 CFR 1.17 (c). A check in the amount of $110 is enclosed as payment for the requested extension of time.

REAL PARTY IN INTEREST

Sony Corporation is the real party in interest by reason of an assignment of the parent of this application from the inventors to Sony Corporation.

RELATED APPEALS AND INTERFERENCES

On information and belief, there are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the decision of the Board of Patent Appeals and Interferences in the instant appeal.

STATUS OF THE CLAIMS

This application is a continuation of U.S. application 09/086,788; and by reason of the Preliminary Amendment filed concurrently with this continuation, claims 19-24 were submitted for examination.

In response to the July 21, 2000 rejection of claims 19-24, claims 19 and 22, the only independent claims in this continuation, were amended.

The next Office Action issued on January 31, 2001 and was a Final Rejection of the amended claims. Appellants responded by arguing against the Final Rejection. No amendments to the claims were submitted.

In the Advisory Action of October 2, 2001, the Examiner stated that the response to the Final Rejection would not be entered because "they raise new issues that would require further consideration and/or search" and, moreover, "they are not deemed to place the application in better form for appeal." The Examiner maintained his rejection of claims 19-24.

Accordingly, the status of the claims is as follows:

Claims allowed: none.

Claims rejected: claims 19-24.

Claims objected to: none.

STATUS OF AMENDMENTS

Amendments were made to claims 19 and 22 in the Amendment filed November 14, 2000. No amendments were submitted in response to the Final Rejection, notwithstanding the assertion that the response to the Final Rejection would not be entered because "they raise new issues that would require further consideration and/or search."

SUMMARY OF THE INVENTION

This invention is directed to a memory card having the electronic configuration shown in Fig. 2 of the present application and operable in accordance with the flow charts illustrated in Figs. 5 and 6. The memory card is used with external apparatus, referred to in this Appeal Brief as a host, which controls the memory card to write data into or erase data from or read data from that memory card (specification page 6, line 12 through page 7, line 4; page 9, lines 14-19). Accordingly, the memory card includes a flash memory 22 (see Fig. 2) which stores the data written from or read by the host. To prevent data in the flash memory from being overwritten, or erased, a switch 23, known as a write protect switch or a write inhibit switch or an erroneous erase prevention switch, is provided (see Figs. 2, 7 and 8).

Data is communicated between the memory card and the external apparatus via an interface including electrical connectors (shown in Fig. 2) and a serial/parallel-parallel/serial interface sequencer (or S/P & P/S sequencer) 31.

A control IC 21 cooperates with instructions transmitted from the external apparatus (or host) to write data to the flash memory. The control IC includes, inter alia, a

command generator 35 which communicates with the host to let the host know if the memory card is "busy." The flow charts shown in Figs. 5 and 6 depict the interaction between control IC 21 and host 1. This interaction is an important feature of the present invention. First, a read status instruction is sent from the external apparatus to the memory card. In response to this read status instruction, the state of switch 23 is sensed. Then, the state of switch 23 is transmitted back to the external apparatus. This switch may be in an inhibit state, which inhibits the writing of data into the flash memory, or an enable state which permits data to be written into the flash memory. If the state of the switch (as received by the external apparatus) is not the inhibit state, the external apparatus sends to the memory card both a write instruction signal (which instructs the memory card to write data to the flash memory) and the data itself. So, four separate instructions or signals must be communicated: (1) the read status instruction must be sent from the external apparatus to the memory card; (2) the state of the switch must be returned to the external apparatus following the read status instruction; (3) the write instruction signal must be sent from the external apparatus to the memory card if the state of the switch, as returned to the external apparatus, is not the inhibit state; and (4) the data to be written must be sent to the memory card if the state of the switch is not the inhibit state and if the write instruction signal has been sent.

The present invention also is directed to a system formed of the aforementioned memory card in combination with the external apparatus. The external apparatus includes a controller (see the CPU 17 in Fig. 1) that performs the functions of transmitting the read status instruction to the memory card and then, if and only if the state of switch 23 is not the inhibit state, transmitting to the memory card both the write instruction and the data to be written (see the flow charts of Figs. 5 and 6).

An advantageous feature of the present invention is to avoid unnecessary and time consuming transmission from the host to the memory card of a write instruction and data to be written if the memory card is not in a condition to write that data. Rather, in this invention, by first transmitting the read status instruction from the host to the card, the status of switch 23 first is determined. If the switch status is "inhibit," the write instruction and the data are not sent to the memory card. This is an improvement over prior art arrangements in which the write instruction and the data are sent to the memory card irrespective of the status of a write protection switch; and then it is up to the memory to ignore the write instruction if the write protection switch is ON.

THE ISSUES

The issue presented in this Appeal is whether Appellants' claims 19-24 are obvious under 35 USC 103 in view of the cumulative teachings of Robinson (U.S. Patent No. 5,428,579) and Komatsu (U.S. Patent No. 5,802,551)[1].

GROUPING OF THE CLAIMS

For the purpose of this appeal, claims 19-24 do not stand or fall altogether. Claims 19-21 constitute one group and claims 22-24 constitute a second group. The patentability of claims 22-24 is not dependent solely upon the patentability of claims 19-21.

ARGUMENT

Claims 19, 20, 22 and 23 were rejected under 35 USC 103 as being obvious in view of the combination of Robinson and Komatsu. Claims 21 and 24 were rejected as being obvious over this combination when further combined with Jigour.[2] Claims 19-24 are set out in the Appendix.

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[1] The Examiner relied upon U.S. Patent No. 5,815,426 (Jigour) in the rejections of dependent claims 21 and 24.

[2] The primary rejection that is addressed here is the rejection based upon the combination of Robinson and

Robinson describes a memory card 110 having a write protect switch 116 which, when in one position, causes "the card control logic of flash memory card 110 [to] prevent[] any writing of data to the flash EPROMs of flash memory card 110" (column 6, lines 15-19). Memory card 110 is coupled to a host computer (i.e. to external apparatus) via an electrical connector. A card control logic 150 oversees the sending out to host computer 101 of status information regarding flash memory card 110 (column 12, lines 47-48). Depending upon the inputs to card control logic 150 from the host computer, the host computer can read the contents of components management registers 111, one of which is a write protection register 457 (column 12, lines 60-66 and column 16, lines 34-38). If bit zero at address 4104 of write protection register 457 is a "1" then the corresponding block in the memory is write protected (column 22, lines 44-51). The sequence by which the memory card is placed in its active mode is described at column 31, lines 9-55. This description, however, is not suggestive of the sequence that is used to write data to the flash EPROMs. As best can be determined, data is supplied from the host computer to the memory card to be written into the flash EPROMs irrespective of the content of write protection register 457. If it turns out that a "1" is stored in the write protection register, which will occur if the write protect switch is set to one particular position, then the data that has been supplied to the memory card will not be written to the flash EPROMs. But this is a function performed by the card control logic. Data will be sent from the host to the memory card no matter the content of the write protection register. This argument was presented during the prosecution of the instant application, and particularly in response to the initial Office Action; and was agreed to by the Examiner. Consequently, it is fair to say that

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Komatsu. Jigour was relied upon for an alleged teaching of transmitting data in serial form. The patentability of the present invention is not premised upon transmitting data in serial form.

Robinson fails to describe the following functions of the "control means" specified in claims 19 and 22:

(1) "said control means sending to said external apparatus... the state of said switch ***in response to a read status instruction transmitted thereto***... from said external apparatus";

(2) "said control means receiving from said external apparatus data to be written to said flash memory and a write instruction signal ***only if the state of said switch that is sent to said external apparatus*** is not said state which inhibits writing."

Stated otherwise, and as agreed to by the Examiner, Robinson does not send data to be written only if, in response to a read status instruction, the memory card returns to the host computer the enable status of write protect switch 116. Apparently, there is no description in Robinson related to the interaction, if any, between the transmission of data and a write instruction from the host computer to the memory card, and the sending of the status of the write protect switch from the memory card to the host computer when the host computer asks for that status.

Komatsu also describes a flash memory to which data is written and from which data is read by a host computer. Data that is supplied to Komatsu's flash memory first is written to SRAM 23 (Fig. 1) and then, if there is room in the flash memory for this new data, that data is transferred from the SRAM to an available sector in a block (column 3, lines 43-55 and column 5, lines 3-5 and 25-47). If the flash memory is filled such that there is insufficient remaining capacity to store the data waiting in the SRAM, the flash memory undergoes a clean up operation which evacuates old data from a block. Then, the new data is written into that cleaned up block (column 5, lines 48 to column 7, line 31). The flow chart shown in Figs. 5-9 of Komatsu

represent the steps performed by processor 22 in writing data to the flash memory, and evacuating and cleaning up the flash memory. According to the clean up operation, data is transferred from a block in the flash memory to SRAM 23 and then that data is rewritten into the flash memory. But, as pointed out at column 6, lines 25-31, before the transferred data is rewritten, the processor first goes to step S30. Here, a search for a write-enable sector is started, beginning with the sector indicated by the Write Pointer. Then, the existence of a write-enable sector is checked at step S31. If there is a write-enable sector, the processor goes to step S32 which moves the data stored in SRAM 23 to the flash memory. Komatsu does not describe what is used to indicate the existence of a write-enable sector. Nor does Komatsu describe how the existence of a write-enable sector is checked. Indeed, Komatsu does not explain how step S31 is carried out.

In applying Komatsu to the claims of the instant application, the Examiner asserted that once Komatsu clears his check on the existence of a write-enable sector, the data and write instructions are passed to the flash memory. This is depicted in the flow chart of Fig. 7 (instructions S30 and S31) and the flow chart in Fig. 9 (instructions S46, S47 and S48) and is described at column 7, lines 14-19.

It is undisputed that Komatsu does not describe any element or feature that is analogous to a write protect switch. While Komatsu mentions the need to find a write enable sector in order to "move data in SRAM to flash memory," there is no hint or suggestion that a write enable sector will or will not be found if a write protect switch happens to be set to an "inhibit" state. Nor is there any hint or suggestion that a write enable sector will or will not be found if a write protect switch is set to an "enable" state. It is submitted, however, that this is the very least suggestion needed to support the conclusion that the claims of the instant application

are obvious. But, Komatsu's write enable sector appears to be merely an indication that there is sufficient storage capacity in a sector to store new data written thereto.

From a fair interpretation of Komatsu, it is evident that, when a host computer wishes to transfer data to Komatsu's memory card 20, that data is supplied to the card's SRAM 23, irrespective of the "status" of the card itself. Then, once the flash memory is sufficiently cleaned up (i.e. it is provided with sufficient storage capacity), the data that had been transferred to SRAM 23 is further transferred to the cleaned up flash memory. There is nothing in Komatsu that would suggest to one of ordinary skill in the art that the host computer first sends to memory card 20 a "read status instruction", and then the memory card returns to the host computer the status of an inhibit switch, and then if the host computer is apprised of the fact that the inhibit switch is not ON, then and only then is data supplied from the host computer to the card.

The Cumulative Teachings of Robinson and Komatsu
Are Not Suggestive of Sending the Status of a
Write Protect Switch in Response to a Read Status Instruction
and Then Receiving Data and a Write Instruction Signal
Only If the Sent Status Is Not an
Inhibit Status

Claims 19-21

Claims 19-21 stand rejected as being obvious in view of the combination of Robinson and Komatsu (Jigour was added to this combination to reject claim 21; but the Examiner relies upon Jigour solely for an asserted teaching of serial transmission of data). Assuming, for the purpose of this argument, that Robinson and Komatsu are properly combinable, it is axiomatic that, to support the Examiner's rejection, the resultant teachings of this combination still must describe all of the elements of, for example, independent claim 19. *In re Sernaker*, 217 USPQ 1, (Fed. Cir. 1983); *Panduit Corp.* v. *Dennison Mfg. Co.* 227 USPQ 337 (Fed. Cir. 1985). This, however, clearly is not the case.

The Examiner agrees that Robinson fails to describe control means included in memory card 110 that cooperates with external apparatus (i.e. a host computer) to execute the following sequence defined by claim 19:

first, sending "a read status instruction" from the external apparatus to the memory card;

second, transmitting to the external apparatus, in response to the read status instruction, the status of the write inhibit switch included in the memory card; and

third, transmitting from the external apparatus to the memory card data to be written, along with a write instruction signal, "only if the state of said switch that is sent to said external apparatus is not said state which inhibits writing."

Indeed, in the Final Rejection here under appeal, the Examiner admits (page 3, lines 5-7 of that Final Rejection) that Robinson "fails to specifically teach the flash memory receiving the data and write instruction signal only after the state of the switch is found by the external apparatus as being in inhibition mode" (emphasis added). But, contrary to the Examiner's conclusion, Komatsu does not provide this teaching.

The Examiner contends that Komatsu is evidence that "it is well known in the art to have such a method when writing to a flash memory." That is, the Examiner contends that Komatsu describes a memory card that receives data and a write instruction signal from the host computer only after the state of a write inhibit switch in the memory card, as sent to the host computer in response to a read status instruction from the host computer, is found by the host computer to be OFF. This contention is not supported by the clear teachings of Komatsu. Komatsu does not describe a write inhibit switch. It would be improper, then, to conclude that one who reads and understands Komatsu would conclude that Komatsu sends the state of this

non-existent switch to the host computer in response to a status inquiry from the host. While Robinson does describe a write inhibit switch, the status of this switch is not sent to a host computer. Why, then, in the absence of any teachings, would it be obvious to one of ordinary skill in the art to transfer to a host computer the state of a write inhibit switch as a prerequisite before any data is transferred from the host to the memory card? The only suggestion in the documents of record to do this is found in the instant application. It is impermissible hindsight to use Appellants' own teaching to reconstruct the prior art in a manner not suggested by either prior art reference. *In re Geiger*, 2 USPQ 2d, 1276 (Fed. Cir. 1987) (Obviousness cannot be established by combining the teachings of the prior art to produce a claimed invention, absent some teaching, suggestion or incentive supporting the combination.... At best in view of these [prior art] disclosures, one skilled in the art might find it obvious to try various combinations of these known [agents]. However, this is not the standard of 35 USC 103); *In re Rouffet*, 149 F.3d 1350 (Fed. Cir. 1998); *Uniroyal* v. *Redkin-Wiley*, 5 USPQ 2d 1434, 1438 (Fed. Cir. 1988) (It is impermissible to use the claims as a frame and the prior art references as a mosaic to piece together a facsimile of the claimed invention). *Lindemann Machinenfabrik GmbH* v. *American Hoist & Derrick Company*, 221 USPQ at 489 (The mere fact that a device utilizes a known scientific principle does not alone make that device obvious). *Orthopedic Equipment Co., Inc.* v. *United States*, 217 USPQ 193-199 (Fed. Cir. 1983) (It is wrong to use the patent in suit as a guide through the maze of prior art references, combining the right references in the right way so as to achieve the result of the claims in suit. Monday morning quarterbacking is quite improper when resolving the question of nonobviousness in a court of law). *In re Gordon*, 221 USPQ 1125, 1127 (Fed. Cir. 1984) (The mere fact that the prior art could be so modified would not

have made the modification obvious unless the prior art suggested the desirability of the modification).

In the Final Rejection of January 31, 2001, the Examiner opined why, in his view, it would be obvious to modify Komatsu so that data would be sent to memory card 20 from the host computer only when the memory card is detected to be write-enabled, that is, so that data would be transferred from the host computer only if a write-enabling switch or signal is detected: "This would prevent data from being unnecessarily transferred from an external device to the card, only to find the write-protect in effect, and have to travel back to the external device" (page 3, lines 12-16 of the Final Rejection). But this purported suggestion of modifying Komatsu is not found in Komatsu or in Robinson. Rather, this suggestion was made by Appellants in their amendment filed November 14, 2000 ("from a clear reading of Robinson, a write instruction is sent to the card, regardless of whether the write protect switch is sent; and it is up to the card controller to determine whether or not the data that is received from the host is written into the card memory. That is, if the write protect switch is not set, data is sent to the card and that data is written into the card memory. But, if the write protect switch is set, data is still sent to the card, but now, that data is not written.") (See page 4, last line to page 5, line 5 of that Amendment.) Appellants agree that it certainly would improve the memory card of Komatsu if data is not transferred from the host computer to SRAM 23 unless and until the host computer sends a status request to the memory card and receives from the memory card a signal indicating that the memory card is in condition to write that data to the flash memory. But Komatsu is not cognizant of such an improvement. To conclude otherwise is, once again, using the hindsight gleaned from Appellants' own disclosure to modify the prior art in a way that the prior art does not contemplate. "The mere fact that [Komatsu] could be so modified would not have made the

modification obvious unless the prior art suggested the desirability of the modification." *In re Laskowski*, 10 USPQ 2d 1397, 1398 (Fed. Cir. 1989). See also *In re Bond*, 15 USPQ 2d 1566, 1569 (Fed. Cir. 1990); *In re Rijckaert,* 28 USPQ 2d 1955, 1957 (Fed. Cir. 1993). *Ex parte Obukowicz*, 27 USPQ 2d 1063, 1065 (PTO Bd. Pat. App. & Int. 1992).

The logical and straightforward result that is obtained by combining the Robinson and Komatsu references is a memory card having a write inhibit switch, such as described by Robinson, and further having an SRAM to which data is transferred from the host computer whenever a write operation is to be carried out, this data being temporarily stored in the SRAM until the flash memory of the memory card is cleaned up, as described by Komatsu. Data from the host computer will be transferred to the SRAM in this reconstructed memory card irrespective of the state of Robinson's write inhibit switch. Indeed, in the reconstructed memory card, the state of the write inhibit switch has no bearing on whether data is transferred to the memory card from the host computer. Data always will be transferred to the SRAM, regardless of the state of the write inhibit switch, and data will remain in the SRAM until the flash memory of the memory card is cleaned up. The reconstructed prior art will not prevent data from being sent to the memory card from the host computer if the state of the write inhibit switch, as sent to the host computer in response to a read status instruction, is ON. On the contrary, however, this is specifically defined by Appellants' claim 19.

It is, therefore, urged that the cumulative teachings of Robinson and Komatsu fail to disclose the "control means" of claim 19, which:

> "send[s] to said external apparatus... the state of said switch in response to a read status instruction transmitted thereto... from said external apparatus" and
>
> "receive[s] from said external apparatus data to be written into said flash memory and a write instruction signal only if the state of said switch that is sent to said external apparatus is not said state which inhibits writing."

Therefore, one of ordinary skill in the art, after reading and understanding Robinson and Komatsu would not be enabled by these references to make and use the memory card specifically defined by claim 19. Consequently, the Final Rejection of claim 19 should be reversed.

Claims 20 and 21 depend from claim 19 and, therefore, these dependent claims include the same "control means" recited by the independent claim. It follows, then, that if claim 19 is unobvious in view of Robinson and Komatsu, dependent claims 20 and 21 likewise are unobvious.

Claim 21 was rejected as being obvious in view of the combination of Robinson, Komatsu and Jigour. Jigour was cited for its asserted teachings of transmitting data to and from a memory device in serial form. The Examiner correctly did not assert that Jigour describes transmitting to an external apparatus the state of a write inhibit switch in response to a read status instruction received from the external apparatus and then, only if the state of that switch is not the "inhibit" state, supplying from the external apparatus data to be written along with a write instruction signal. Consequently, the aforenoted deficiencies of Robinson and Komatsu are not cured by Jigour. Claim 21 therefore is patentably distinct over the prior art relied upon by the Examiner.

Claims 22-24

Claim 22 recites the very same "control means" of claim 19; and this alone distinguishes claim 22 from the cumulative teachings of Robinson and Komatsu. In addition, claim 22 recites the further limitation of "a controller" in the external apparatus which transmits the read status instruction to the memory card to determine whether a data writing operation is inhibited, and then transmits to the memory card the data to be written and also the write

instruction if and only if the state of the write inhibit switch, as sent from the memory card to the external apparatus in response to the read status instruction, is not the inhibit state. Not only do Robinson and Komatsu fail to describe the "control means" in the memory card that is recited by claim 22, but these references also fail to describe the "controller" in the external apparatus that is defined by this claim. Therefore, in view of the legal authorities discussed above, it is urged that claim 22, together with claims 23 and 24 dependent thereon, is unobvious and is patentably distinct over the prior art references particularly relied upon by the Examiner in his Final Rejection.

Accordingly, is respectfully requested that the rejection of claims 22-24 as being obvious be reversed.

CONCLUSION

The Examiner has improperly rejected claims 19-24 as being obvious in view of Robinson and Komatsu (and Jigour). As is clear from the authorities discussed above, the failure of each of these references to describe a critical element recited in the claims cannot be cured by using the hindsight gleaned from Appellants' disclosure to supply that missing element. The logical result obtained from combining these references produces a structure that is patentably different from that specified by Appellants' claims.

This Honorable Board is respectfully requested to reverse the Examiner's rejection of claims 19-24. It is further requested that this Board find claims 19-24 to be nonobvious, within the meaning of 35 USC 103.

Respectfully submitted,

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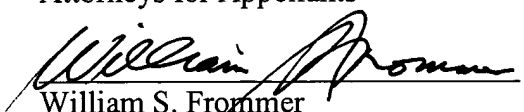

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APPENDIX

CLAIMS ON APPEAL

19. A memory card for storing data transmitted from an external apparatus, said memory card comprising:

a flash memory for storing said data transmitted from said external apparatus;

a switch settable to a state which inhibits writing data into said flash memory;

an interface for transmitting data to and receiving data from said external apparatus; and

control means for controlling said memory card in accordance with an instruction transmitted from said external apparatus, said control means sending to said external apparatus via said interface the state of said switch in response to a read status instruction transmitted thereto via said interface from said external apparatus and said control means receiving from said external apparatus data to be written to said flash memory and a write instruction signal only if the state of said switch that is sent to said external apparatus is not said state which inhibits writing.

20. A memory card as claimed in claim 19, wherein said interface includes nine connectors at least one of which transmits and receives data.

21. A memory card as claimed in claim 19, wherein said data is received from and transmitted to said external apparatus in serial form.

22. A system comprising a memory card and an external apparatus, wherein data is communicated therebetween,

said memory card comprising:

a flash memory for storing said data transmitted from said external apparatus;

a switch settable to a state which inhibits writing data into said flash memory;

an interface for transmitting data to and receiving data from said external apparatus; and

control means for controlling said memory card in accordance with an instruction transmitted from said external apparatus, said control means sending to said external apparatus via said interface the state of said switch in response to a read status instruction transmitted thereto via said interface from said external apparatus and said control means responding to a write instruction received from said external apparatus via said interface to write into said flash memory data received from said external apparatus;

and said external apparatus comprising:

a controller for writing data to or erasing data from the flash memory of said memory card, said controller transmitting a read status instruction to said memory card via said interface to determine whether a data writing operation to the flash memory of said memory card in inhibited and said controller transmitting via said interface said write instruction and said data to be written into said flash memory after said external apparatus receives said state of said switch and only if said state is not the state that inhibits writing.

23. A system as claimed in claim 22, wherein said interface includes nine connectors at least one of which transmits and receives data.

24. A system as claimed in claim 22, wherein said data is received from and transmitted to said external apparatus in serial form.